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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/621,044 | 07/15/2003 | Nadine Collaert | IMEC280.001AUS | 8902 |

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| EXAMINER | |
|---|---|
| DANG, TRUNG Q | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2823 | |

DATE MAILED: 12/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/621,044 | COLLAERT ET AL. | |
| | Examiner | Art Unit | |
| | Trung Dang | 2823 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-33 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-33 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 15 July 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 10/17/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 14-18, 20, 25, 27-33 are rejected under 35 U.S.C. 102(b) as being anticipated by Chapman et al. (US 6,118,161 cited by applicants).

The reference teaches the claimed invention in that it discloses a method of forming a FinFET device comprising:

providing an SOI substrate 102 comprising a semiconductor layer 106;

forming a plurality of active areas, insulated from each other by field areas 114, on the semiconductor layer (col. 6, lines 45-67);

forming a disposable gate 134 (corresponding to the claimed dummy gate) on the active area (Fig. 22 and col. 4, lines 51-60);

forming source/drain regions 110/112 within the active area, the source and drain regions being self aligned to the disposable gate 134 (col. 4, lines 60-65);

covering the substrate with an insulating layer 114 so as to leave the disposable gate 134 exposed (Fig. 12);

patterning the exposed disposable gate 134 and the semiconductor layer 106 so as to create an open cavity 118 in the insulating layer 114 and in the

semiconductor layer and to form a dummy fin comprising layers 130, 132 and a semiconductor fin 108 aligned to the dummy fin in the cavity, both of the fins extending from the source region 110 to the drain region 112, thereby exposing the semiconductor layer 106 (Fig. 15 and related text).

For claim 14, the device illustrated in Fig.8 is considered as a planar FET because as shown in the figure drawing the device including the gate 116 and isolation 114 is substantially planar.

For claims 15-16, see col. 4, lines 55-57 for the stack including at least one of an oxide (dielectric) layer, a polysilicon (conductor) layer, and a nitride layer.

For claims 27 and 30, col.3, lines 25-28 compares the drive current in the strip channels with that of a standard bulk CMOS transistor, hence it is believed that the reference includes the manufacture of a CMOS device. And a CMOS device includes a p-type FET and an n-type FET.

For claim 31, see col. 3, line 42 for the dimension of channel width 108.

For device claims 17, 18, 20 and 25, the process as described above produces every element of the structure as claimed.

## *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-13, 19, and 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chapman et al. as above in view of Fried et al. (US 6,583,469).

Chapman teaches a method of forming a FinFET as described above. Chapman differs from the claims in not disclosing the step of forming spacers against the sidewalls of the cavity 118 prior to forming gate electrode 116 (see Fig. 17).

Fried teaches a method of forming FinFET device, which includes the formation of spacers 58 against sidewalls of a cavity defined by isolation 52, depositing gate material 32 in the cavity, and planarizing the gate material until the isolation 52 is exposed (Figs. 29B-30A and related text).

It would have been obvious to one of ordinary skill in the art to modify Chapman's process by forming spacers against sidewalls of cavity 118 as suggested by Fried because the spacers would provide isolation between source/drain and gate electrode, hence reducing short channel effect.

For claims 8 and 9, see Fig. 16 in Chapman, wherein layers 132 and 130 of the stack are removed.

For claims 10 and 12, see Figs. 15B-17B in Fried for the teaching of

depositing gate dielectric layer 30 of a silicon nitride (col. 6, lines 30-32), depositing gate electrode material, and planarizing the layer of gate dielectric and the layer of gate electrode material until the insulating layer 20 is exposed. Note that silicon nitride is a high-k dielectric material compared to silicon oxide.

For claim 11, see col. 6, lines 4-10 in Chapman for the teaching of patterning the gate dielectric and gate electrode material to form a T-gate structure.

For device claims 19-24, each of the process explained above produces the structure as claimed.

3. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chapman as above in view of Noble et al. (US 6,107,663).

Chapman teaches a CMOS circuit including FinFET devices as explained above. Chapman differs from the claim in not disclosing that the CMOS circuit comprises a CMOS inverter.

Noble teaches a CMOS circuit having a fin structure comprises an n-type FET and a p-type FET. The n-type FET and p-type FET are configured in such a way to form a CMOS inverter (Fig. 1A). It would have been obvious to one of ordinary skill in the art modify Chapman's teaching by configuring n-type FET and p-type FET in a manner taught by Noble so as to form an inverter because such is known in the art, and the application of a known technique to made the same would have been within the level of an artisan.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trung Dang whose telephone number is 571-272-1857. The examiner can normally be reached on Mon-Friday 9:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trung Dang
Primary Examiner
Art Unit 2823

12/13/04